Appl. No.: 09/785,143
Amdt. dated April 19, 2004
Reply to Office action of February 5, 2004

Amendments to the Specification:

Please replace the paragraph beginning at page 5, line ~~29~~ 19, with the following rewritten paragraph:

Figure 3 illustrates a block diagram of one embodiment of a portion of the computer of Figure 1; and

Please replace the paragraph beginning at page 12, line 14, with the following rewritten paragraph:

Vectorization techniques, including loop distribution and strip mining, have been used in compilers for vector processors and are known to those skilled in the art. However, these vectorization techniques have been used in the past to improve the performance of vector processors, not to improve cache management of a scalar processor, as describe herein.

Please replace the paragraph beginning at page 14, line 15, with the following rewritten paragraph:

It will be appreciated that the vectorizable memory operations may fall within three general groups. Memory operations that read a vector, memory operations that modify a vector, and memory operations that define a vector are all vectorizable memory operations. However, different cache management instructions may be useful to enhance the operation of the cache, depending on the type of vectorizable memory operation being restructured.

AC 7/5/06